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Design and Simulation Teaching Practice of an N-Base Counter Based on Multisim

Qingjuan Feng
Beijing Information Science and Technology University, Beijing, China

Abstract: To improve the teaching quality of sequential logic circuits in the Digital Electronic Technology course and meet the requirements for cultivating college students' innovation ability under the background of New Engineering, this paper takes the design and simulation of an N-base counter as a teaching case and explores a teaching mode that combines theoretical teaching with simulation practice. In view of the shortcomings in current experimental teaching, the paper proposes a systematic teaching method of analysis first and simulation verification afterward. First, theoretical analysis is carried out for the three core functional modules of counting, decoding, and display. Second, Multisim software is used to conduct simulation verification of typical counters such as septenary, sexagesimal, and twenty-four-base counters. Different-base counters are formed by changing the connections between chips and peripheral circuits, so that the simulation results are consistent with the theoretical analysis. This teaching method can effectively stimulate students' learning interest and deepen their understanding and mastery of the analysis and design of arbitrary-base counters. By transforming abstract theoretical knowledge into intuitive simulation results, the teaching effect and quality are significantly improved.

Keywords: N-Base Counter; Simulation; Teaching Practice

1. Introduction

Digital Electronic Technology is an important professional basic course in electrical engineering, automation, electronics, information technology, and related fields in higher engineering institutions, and it is also one of the fastest developing disciplines at present. The teaching purpose of this course is to enable students to master the basic theories, basic knowledge, and basic skills of digital circuits, and to cultivate their ability to analyze and solve problems. Digital circuits are mainly divided into combinational logic circuits and sequential logic circuits, among which sequential logic circuits are one of the core contents of the course. As a typical and widely used medium-scale device in sequential logic circuits, a counter can not only count clock pulses, but also be used for digital operations such as frequency division, timing, and pulse generation [1,2]. Therefore, learning counters requires students not only to have analytical ability, but also to master design methods. In real life, counters of various bases are widely used; for example, a week often uses a septenary system, and time often uses a duodecimal or twenty-four-base system. However, there are currently relatively few common types of counters, and the most commonly used ones are decimal and hexadecimal counters. Therefore, designing arbitrary-base counters is particularly necessary. It has also always been a key and difficult point in teaching, and traditional classroom lecturing makes it difficult for students to establish intuitive understanding.

At the same time, information technology is promoting profound reforms in traditional educational concepts and methods. How to deeply integrate information technology with classroom teaching of Digital Electronic Technology, make full use of information resources and tools to design the teaching process reasonably, encourage students to take the initiative in inquiry and practice, and improve classroom efficiency has become an important research topic [3-5]. For the topic of arbitrary-base counter design, which is rich in content but difficult for students to understand and apply, this paper adopts a teaching method of theoretical design plus software simulation. With the design of an N-base counter as the goal, and around the three key links of counting, decoding, and display, Multisim software is used for circuit simulation. This applies learned

knowledge to practice, improves learning efficiency, saves experimental costs, stimulates students' learning interest, and effectively solves the key and difficult points of teaching.

2. Teaching Objectives and Key Teaching Points of the N-Base Counter

The goals of teaching the N-base counter are to help students learn the basic knowledge and construction methods of sequential logic circuits in an orderly way. There are five particular teaching goals. First, students need to grasp the basic concepts; they should be able to distinguish between sequential logic circuits and combinational logic circuits, and learn about clock signals, states, etc. Secondly, they should be proficient in the design method; that is to say, they need to master the basic rules for applying the clear method and the preset method, which are two typical ways to design N-base counters, and be able to choose a suitable design plan based on different counting needs. Thirdly, they should be able to. Familiar with chip characteristics: they should be familiar with the function table and external pin characteristics of the counter chip 74LS160, including the correct connection and use of the clock input, clear terminal, preset terminal, enable terminal, and output terminals. Fourth, they should learn module division: they should learn the functional division and cascade relationship of the three key modules of counting, decoding, and display. Fifth, they should acquire independent design ability: given any value of N, they should be able to independently design an N-base counter circuit, complete circuit construction and simulation debugging in Multisim, verify the correctness of the logic function, and cultivate engineering practice ability and problem-solving ability.

Around the above teaching objectives, the key teaching points of the N-base counter mainly include four parts. First is the design method of the N-base counter. With the 74LS160 chip as the core, the design ideas and implementation steps of the clear method and the preset method are emphasized. The clear method is suitable for feedback clear control and has a simple circuit structure, while the preset method is more flexible and can implement arbitrary-N counting, especially for noncontinuous counting. Second is the implementation of the decoding and display modules. The decoding and display modules are used to complete the conversion from BCD code to a seven-segment digital tube. The matching rules between the decoder and common-anode or common-cathode digital tubes are clarified, and the selection method of current-limiting resistors is mastered to ensure that the counting results can be displayed intuitively and stably, avoiding display flicker or error codes. Third is the cascading and debugging of the three functional modules: the counting, decoding, and display modules are cascaded. Students are required to correctly connect circuits at all levels, Understand the signal flow and timing, learn basic debugging methods, know how to troubleshoot faults, and be able to solve common problems independently, such as abnormal display and counting jumps. Fourthly, there is Simulating software with Multisim. A whole N-base counting circuit is constructed in the Multisim simulation environment, and then the whole process is simulated. Theoretical design to simulation verification is completed. Emphasis is placed on cultivating students' ability to use virtual instruments such as oscilloscopes for signal testing and result analysis, and on familiarizing them with component library calling, circuit wiring, and simulation operation, laying a solid foundation for subsequent actual hardware experiments.

3. Basic Constituent Modules of the N-Base Counter

An N-base counter is a general type of sequential logic application system. The first purpose is to accumulate the number of input clock pulses and then show the counted amount in decimal digital form. To achieve the above function, the three main parts of a system are typically the counting module, the decoding module and the display module. The three modules together can complete the whole signal conversion process of pulse input to binary code and then to digital display.

3.1 Counting Module

The counting module is the main part of the N-base counter. It is to count the input clock pulses and then output the corresponding binary code or BCD code. The 74LS160 is the basic counter chip used in this paper. It is a synchronous decimal counter with many functions, such as asynchronous clear, synchronous load, and several enable controls, and is very suitable for the design of N-base counters. The pin diagram

of the 74LS160 chip is shown in Figure 1, and the pin function description and logic function table are shown in Table 1 and Table 2.

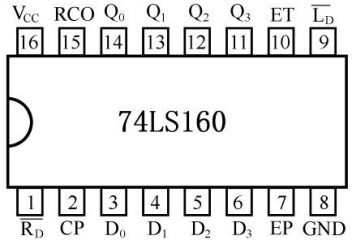

Figure 1. Pin Diagram of 74LS160

There are two implementation methods for N-base counters: the preset method and the clear method. The preset method is implemented by using the preset terminal of the counter. First, an initial value is set, which is not necessarily 0. When the counter counts to a specified state, usually the maximum value, the decoding circuit sends a load signal and reloads the preset initial value into the counter, so that the counter skips invalid states and cycles through only N valid states. The preset method is highly flexible and can implement arbitrary-base counting within any counting range.

Table 1. Pin Function Description of 74LS160

Pin	Function Description
D_0-D_3	Input terminals (initial value is zero)
EP	Operating-state terminal
ET	Operating-state terminal
$\overline{L_D}$	Load terminal
$\overline{R_D}$	Clear terminal
CP	Pulse input terminal
Q_0-Q_3	State output terminals
RCO	Carry terminal

Table 2. Logic Function Table of 74LS160

input							output						
$\overline{R_D}$	$\overline{L_D}$	CP	EP	ET	D3	D2	D1	D0	Q3	Q2	Q1	Q0	RCO
0	×	×	×	×	×	×	×	×	0	0	0	0	0
1	0	↑	1	1	d	c	b	a	d	c	b	a	0
1	1	↑	0	0	×	×	×	×	unchanged	0			
1	1	↑	1	1	×	×	×	×	count	0			
1	1	↑	1	1	×	×	×	×	1	0	0	1	1

The clear method is implemented by using the clear terminal of the counter. In design, when the counter starts from the initial state, usually 0, and counts to the Nth state, the decoding circuit detects this state and immediately generates a clear signal, making the counter jump back to state 0 and restart counting. In this way, the valid states are 0 to N-1, for a total of N states. It should be noted that the action time of the clear signal is extremely short, and the difference between asynchronous and synchronous clearing must be considered: asynchronous clearing responds quickly but may produce glitches, while synchronous clearing is more stable but requires clock coordination [6-8].

By comparison, the clear method has a simple circuit, but the initial state is fixed at 0. The preset method is flexible in design and highly reliable, and it can implement arbitrary-base counters with nonzero starting points.

3.2 Decoding Module

The decoding module is responsible for converting the BCD code output by the counting module into the driving signals required by the seven-segment digital tube. This paper uses the HCF4511BE BCD/seven-segment digital tube decoder to implement the decoding function. The core function of this module is code conversion, namely converting a 4-bit binary input into seven outputs, a to g, which respectively control the seven light-emitting segments of the digital tube. The truth-table logic is integrated inside the decoder and can automatically process the display codes for the ten digits from 0 to 9. The stability and correctness of the decoding module are directly related to the accuracy of the display module.

3.3 Display Module

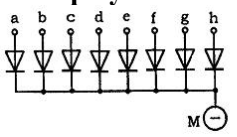

Figure 2. Common-Cathode Structure

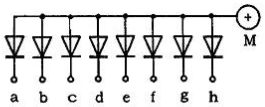

Figure 3. Common-Anode Structure

The display module is composed of seven-segment digital tubes and is used to convert the segment driving signals output by the decoding module into visible numbers. Digital tubes are divided into common-cathode and common-anode types, as shown in Figure 2 and Figure 3. The display module is the final output link of

the system, and indicators such as brightness, response speed, and power consumption affect user experience. This paper tests both common-cathode and common-anode methods.

Through the coordination of the counting, decoding, and display modules described above, the function of the N-base counter can be realized. In teaching, guiding students to understand the functional positioning and cascade relationship of each module is the key to mastering sequential logic system design.

4. Simulation of the N-Base Counter in Multisim

Multisim is a professional electronic circuit simulation and design software launched by National Instruments in the United States. The software mainly uses a graphical interface, is easy to operate, and can directly observe circuit operation results, so it can be used for auxiliary teaching of digital circuits. As a common module of sequential logic circuits in digital circuits, the counter can not only be used for clock pulse counting, but also be widely used in operations such as frequency division, timing, and pulse generation [9,10]. In practical applications, counters of different bases, such as twenty-four-base and sexagesimal counters, are needed. However, the existing counter types are limited, commonly decimal and hexadecimal, so the design of arbitrary-N-base counters has become a common problem in applications. Based on this, this paper intends to introduce the application of Multisim software in the design of arbitrary-N-base counters.

The following are simulation circuit examples of septenary, sexagesimal, and twenty-four-base counters implemented in Multisim simulation software according to the design ideas in Section 3.

The first example is the implementation of a septenary counter, and the designed circuit is shown in Figure 4. The counting module uses the clear method for counting, the clear module is implemented by a three-input NAND gate, and the display module uses a common-cathode connection.

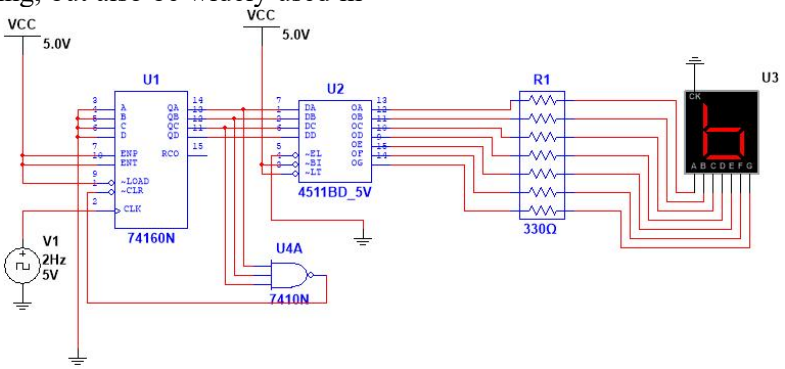

Figure 4. Simulation Circuit Diagram of the Septenary Counter

The second example is the implementation of a sexagesimal counter, and the designed circuit is shown in Figure 5. The counting module uses the preset method for counting, the preset module is implemented by a three-input NAND gate, and both display modules use common-anode connections.

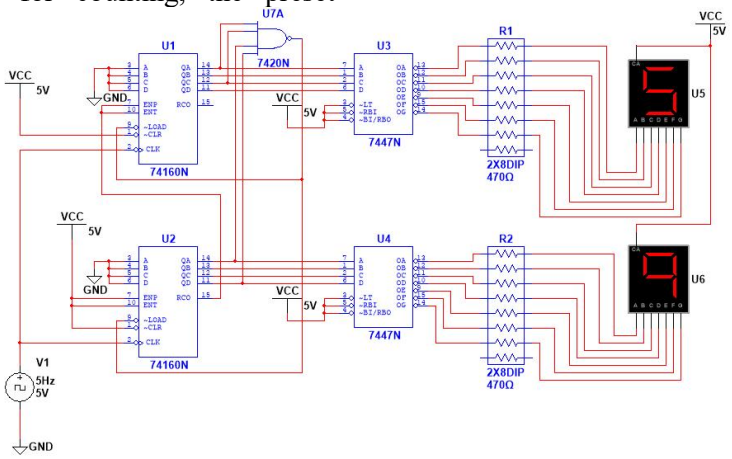

Figure 5. Simulation Circuit Diagram of the Sexagesimal Counter

The third example is the implementation of a twenty-four-base counter, and the designed circuit is shown in Figure 6. The counting module uses the preset method for counting, and the preset module is implemented by a three-input NAND gate. The display module in this example has a built-in decoding function.

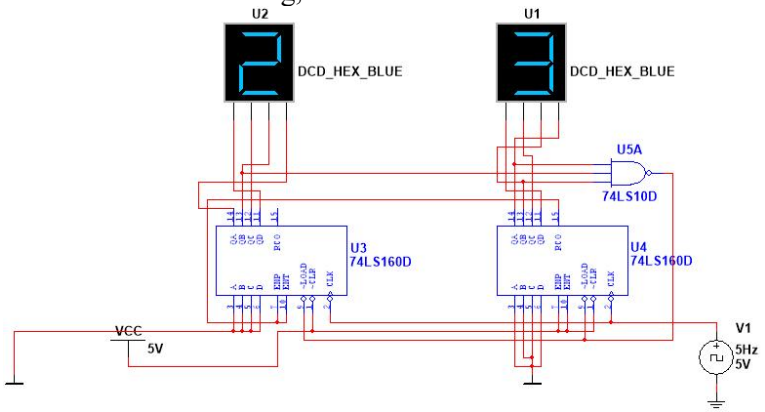

Figure 6. Simulation Circuit Diagram of the Twenty-Four-Base Counter

It can be seen from the three simulation examples above that either the clear method or the preset method can successfully implement the specified N-base counting function. The septenary counter uses the feedback clear method to generate a clear signal in the 0110 state, with Count range: 0 to 6. The sexagesimal counter has two cascaded chips; the units digit is carried over to the tens digit every ten pulses, and when the tens digit reaches 6 and the units digit is 0, feedback clearing is performed to achieve a 0-59 cycle. The twenty-four-base counter is a preset type, and after counting to 24, it can be loaded or cleared. Triggered to complete a 0-23 cycle. The simulation results verify the correctness of counting state transitions, the reliability of the clear and preset counting methods, and the timing coordination of multi-chip cascading. At the same time, digital display and waveform diagrams intuitively present the whole counting process, making it convenient to quickly troubleshoot design errors. This proves the correctness and feasibility of the counting logic design and provides an effective reference for the subsequent design and teaching of more complex sequential circuits.

5. Conclusion

This paper will take the teaching design of the N-base counter as the focus and use theoretical design combined with software simulation as the main path. It is a structured introduction to the functions and cooperation of the three main parts: counting, decoding and displaying. At the theoretical level, it explains in detail the working principle of the counter, the logic design of the feedback clear method and preset method, and the display driving method of the decoder and digital tube. Based on the above, the simulation implementation of the three typical counters, namely septenary, sexagesimal and twenty-four-base counters, will be carried out in the Multisim platform.

Multisim simulation has many advantages over the old way of teaching theories in an introductory course. First of all, it can turn the abstract nature of static timing diagrams in textbooks into dynamic and interactive simulation processes to help students better grasp the concept of clock edge and state transition. Second, it gives a quick answer. At any time, students can change the circuit wiring and chip parameters to observe changes in the results and thus learn about feedback logic and modulus control through trial and error. Third, it can reduce hardware costs and experimental risks; there will be no interference from hardware faults such as chip burnout and poor contact in the teaching, and more students will be able to complete the design task independently. Bourth, it stimulates enthusiasm for active learning. In the simulation environment, students no longer passively receive knowledge, but actively explore implementation schemes for counters of different bases, cultivating innovative thinking and engineering practice ability. Practice proves that this teaching mode effectively improves teaching effect and design efficiency, and provides a feasible path for the reform of the Digital Electronic Technology course under the background of New Engineering.

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